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ABSTRACT OF THE DISCLOSURE

An apparatus comprising a memory, an encoder and one or more registers. The memory may be configured to (i) read and/or write a plurality of state vectors and (ii) read and/or write data. The encoder may be configured to present state vectors to be written in response to (i) data read from the memory (ii) a first address and (iii) a serial data stream. The registers may be configured to present the first address in response to an input address.